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**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Docket Number (Optional)

P7866C

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on July 1, 2009Signature /Christine Hartness/Typed or printed name Christine Hartness

Application Number

10/780,330

Filed

02-17-2004

First Named Inventor

Gilbert Wolrich

Art Unit

2187

Examiner

Prasith Thammavong

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor./Robert A. Greenberg/

Signature

☐ assignee of record of the entire interest.  
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.  
(Form PTO/SB/96)Robert A. Greenberg

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Date

Registration number if acting under 37 CFR 1.34 \_\_\_\_\_

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below\*.

☒ \*Total of 1 forms are submitted.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Wolrich, et al.                      Art Unit : 2187  
Serial No.: 10/780,330                      Examiner : Prasith Thammavong  
Filed : February 17, 2004                      Assignee : Intel Corporation  
Title : MEMORY MAPPING IN A PROCESSOR HAVING MULTIPLE  
PROGRAMMABLE UNITS

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Pre-Appeal Brief Request for Review

Claim 28 recites a processor that integrates multiple programmable units. In particular, the processor includes logic to provide data access to a resource, such as a register, within a first programmable unit to a second programmable unit in response to a data access request of the second programmable unit specifying an address within a single address space. To illustrate by example, as described in the specification, a first programmable unit (e.g., processor core 50) can access internal register locations within other programmable units (e.g., engines 22a-22f) by specifying an address in the address space shown in FIG. 4.

Claim 28 stands rejected as anticipated Tremblay (U.S. 6,212,604). In particular, the Final Office Action mailed 5/12/2009 equates P1 (208 in FIG. 3) and P2 (210) as the recited first and second programmable units. The Final Office Action then equates Tremblay's teaching in col. 4 lines (7-29) with the recited logic. This portion of Tremblay

describes how P1 and P2 can execute the very same instruction but access different memory locations based on settings of index base registers. This section, however, does not describe that P1 can access registers within P2, or that P2 can access registers in P1. In Tremblay, P1 and P2 access their own internal registers, not those of another programmable unit.

The Advisory Action mailed 06/18/2009 advanced a new argument equating col. 2 lines 24-48 of Tremblay with the recited logic<sup>1</sup>. This new argument is particularly terse and Attorney for Applicant cannot state with any confidence what exactly is being equated with the recited "resource". The Advisory Action seems to argue that the shared access of P1 and P2 to instruction cache 212 describes the recitation of claim 28 as described above. However, the description that P1 and P2 both access and execute the same instructions in shared instruction cache 212 does not describe the recited logic to provide data access to a resource, such as a register, within a first programmable unit to a second programmable unit in response to a data access request of the second programmable unit specifying an address within a single address space.

In short, the limitation described above has not been met in Tremblay in the Final Office Action or Advisory Action. Claims 36 and 44 recite similar limitations and were similarly rejected. For the reasons above, these rejections constitute clear error. For at least these reasons, Attorney for Applicant requests withdrawal of the rejection of claims 28, 36, and 44 and their corresponding dependent claims.

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<sup>1</sup> Attorney for Applicant believes the Examiner intended to reference col. 3 lines 24-48.

Applicant : Wolrich, et al.

Intel Docket No.: P7866C

Serial No. : 10/780,330

Filed : 02/17/2004

Response to Final Office Action Mailed 5/12/2009

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For at least the reasons above, Attorney for Applicant respectfully requests  
withdrawal of the rejections.

Respectfully submitted,

Dated: 7/1/2009

/Robert A. Greenberg/

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